

1 IN THE SPECIFICATION

2 Please replace paragraph number 0016 with the following:

3 Although components can be arranged along a column or row of the array of plated
4 vias, the tight spacing in an array in a typical PWB limits the component to being placed
5 diagonally as shown. A component 43 representing, for example, a 0402 size (i.e.,
6 0.04" length_x_0.02" width_x_0.02" height) chip capacitor, shown in the bottom right of
7 Figure 3, is oriented diagonally in a space 42, that is, between the keyhole shaped
8 solder masks 7 and 9. This orientation keeps the conductive trace to a minimal length
9 which minimizes trace inductance causing performance degradation such as group
10 delay, self-resonance with capacitive components or frequency roll off.

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